REMARKS

Concurrently filed herewith is an Excess Claims Fee letter for two additional total claims.

Telephone Interview Dated August 16, 2006

Applicants gratefully acknowledge Examiner Beveridge and Primary Examiner Johnson for taking time from their busy schedule on August 16, 2006, to conduct a telephone interview with the inventors and their representative. The interview was very helpful in advancing prosecution, since it provided the Office the opportunity to explain its position for maintaining the rejections currently of record, when the rejection did not seem to make much sense from a purely technical perspective.

Before discussing the invention itself during the interview, Applicants' representative stated the position of Applicants that the rejection based on 35 USC §112, first paragraph, for claims 10 and 11 should perhaps be best addressed by deleting the wording "substantially simultaneously", since the word "co-dispensing" implies simultaneity, thereby making this descriptive redundant. The Examiners had no comment.

The inventors then summarized the present invention and the technical reasons that the prior art currently of record fails to satisfy the plain meaning of the claim language. Examiner Beveridge responded that she felt that there was indeed patentable subject matter described in the specification but she also felt that the independent claims could still be interpreted as reading on the prior art of record. When pressed further and as best understood, Examiner Beveridge stated that she considers that, in viewing Figure 4A of Kawai from a system perspective, there would be some of the bonding wires that would carry the signal as an input signal and other bonding wires that would correspondingly carry the return signal

Applicants' representative then further probed this interpretation of Kawai, explaining that, for satisfying the initial burden of a *prima facie* rejection, the USPTO would have to be able to point to a specific signal line in Kawai that satisfies the plain meaning of the claim language that, for that specific signal line, there is a plurality of bonding wires providing a controlled impedance effect and this plurality of bonding wires conducts both the signal current and the signal return current, and that it would not appear that this interpretation of the bonding wires 31,32 of Kawai would satisfy the plain meaning of these claim limitations.

Primary Examiner Johnson then stated that he considered that the position of the USPTO was clear, in that bonding wires 31 of Figure 4A of Kawai could be considered as conducting the signal return current and bonding wires 32 could be considered as conducting the signal current, and that Applicants should respond to this interpretation on the record.

Status of the Prosecution

The independent claims are returned to their original wording in preparation for Appeal. New claims 31 and 32 are added, wherein claim 32 explores wording that is perhaps palatable to the Examiner, in addition to the previous wording attempt, now moved to dependent claim 31.

Claims 1-32 are all the claims presently pending in the application. Claims 25 and 26 are withdrawn, pending resolution of the propriety of the restriction requirement, which was timely traversed and which matter will be further pursued once the allowable subject matter of the examined claims is determined.

It is noted that Applicants specifically state that no amendment to any claim herein should be construed as a disclaimer of any interest in or right to an equivalent of any element or feature of the amended claim.

Applicants gratefully acknowledge the Examiner's indication that claims 4, 6, 14, 16, 18, 21, 22, and 28-30 would be allowable if rewritten in independent form. However, Applicants respectfully submit that all of the claims are allowable.

Claims 1-3, 5, 7, 9, 12, 19, 24, and 27 stand rejected under 35 U.S.C. § 103(a) as allegedly unpatentable over U.S. Patent No. 6,084,295 to Horiuchi et al., further in view of US Patent 5,477,083 to Kawai.

Claim 8 stands rejected under 35 U.S.C. § 103(a) as allegedly unpatentable over Horiuchi/ Kawai, further in view of US Patent Publication US 2004/0182911A1 to Chia et al. Claims 10 and 11 stand rejected under 35 U.S.C. § 103(a) as allegedly unpatentable over Horiuchi/Kawai, further in view of US Patent 3,840,169 to Steranko et al.

Claim 13 stands rejected under 35 U.S.C. § 103(a) as allegedly unpatentable over Horiuchi/Kawai, further in view of US Patent Publication US 2001/00154900A1 to Lee.

Claims 15 and 17 stand rejected under 35 U.S.C. § 103(a) as allegedly unpatentable over Horiuchi/Kawai, further in view of US Patent 5,294,897 to Notani et al. Claim 20 stands

rejected under 35 U.S.C. § 103(a) as allegedly unpatentable over Horiuchi/Kawai, further in view of US Patent 4,555,052 to Kurtz et al. Claim 23 stands rejected under 35 U.S.C. § 103(a) as allegedly unpatentable over Notani, further in view of Kawai.

These rejections are respectfully traversed in the following discussion.

I. THE CLAIMED INVENTION

As described and defined in, for example, claim 1, the present invention is directed to a method of making an electronic interconnection. For a signal line to be interconnected, a plurality of bonding wires is used in a configuration that provides a controlled impedance effect.

The conventional method of wire bonding, as described on page 2 of the specification, beginning at line 2, inherently represents a parasitic inductance that limits bandwidth signals when a single bonding wire is used for a signal. This problem has been addressed in various methods, including the use of flip chip and ball grid concepts or filling the transition region with a high dielectric constant material such as an epoxy containing a ceramic. However, these conventional methods are not always applicable and can be expensive to implement.

The claimed invention, on the other hand, introduces into the art the entirely different concept of using a plurality of bonding wires for a specific signal line. By appropriately configuring this plurality of bonding wires, the plurality of bonding wires provides a controlled impedance effect for that specific signal line. In practice, for any given signal connection, a typical configuration might use one bonding wire to carry the signal current and the other bonding wire to carry the return current, which can represent ground for a single ended signal and the complementary signal for a differential pair.

II. THE WITHDRAWAL OF CLAIMS 25 AND 26

The Examiner has made final the restriction for claims 25 and 26. Applicants decline to cancel these claims at this time, since a Petition to withdraw this restriction will be filed once the allowable subject matter of the active claims is established. However, Applicants bring to the Examiner's attention that the record currently fails to reflect a reasonable support for the position

that "lead frame or lead-less plural joint forming can make the electronic product", since it is submitted that the plain meaning of the claim language of independent claim 25 requires that the apparatus have ".... at least one signal line having a plurality of bonding wires configured to provide a controlled impedance effect for said signal line."

That is, the term "bonding wire" is a term of art that cannot be ignored in the restriction requirement analysis and it will be necessary for the USPTO to provide some evidence that such plurality of bonding wires for a single signal line are used in an apparatus. The mere presence of a controlled impedance effect for a signal line would be insufficient evidence to maintain the restriction unless the plain meaning of the claim language is satisfied, wherein it is required that bonding wires be used for the signal line and provide the mechanism for the controlled impedance effect.

III. THE 35 USC §112, FIRST PARAGRAPH, REJECTION

As mentioned above relative to the telephone interview dated August 16, 2006, Applicants submit that the word "co-dispensing" implies simultaneity. Therefore, Applicants have amended claims 10 and 11 to eliminate the wording seemingly at issue. It is noted, however, that Applicants traverse that the specification as-filed fails to support the deleted wording, since claim language is not required to exactly track the wording of the specification (*e.g.*, see MPEP § 2163.02: "*The subject matter of the claim need not be described literally (i.e., using the same terms or* in haec verba*) in order for the disclosure to satisfy the description requirement*").

IV. THE PRIOR ART REJECTIONS

The Examiner alleges that Horiuchi, when modified by Kawai, renders obvious claims 1-3, 5, 7, 9, 12, 19, 24, and 27, and when further modified by Chia, renders obvious claim 8, when further modified by Steranko, renders obvious claims 10 and 11, when further modified by Lee, renders obvious claim 13, when further modified by Notani, renders obvious claims 15 and 17, and when further modified by Kurtz, renders obvious claim 20. The Examiner further alleges that Notani, when modified by Kawai, renders obvious claim 23.

Applicants again submit that there are elements of the claimed invention which are neither taught nor suggested by Horiuchi, Notani, or newly-cited Kawai, when properly interpreted.

First, Applicants submit that the discussion during the above-mentioned telephone interview suggests that there is some confusion related to the Examiner's responsibility, discussed in MPEP §2111, to give the claim language its "broadest reasonable interpretation consistent with the specification." This obligation for broad interpretation is only for the claim language and does not extend to the interpretation of the prior art references. The prior art teaches whatever it teaches, to one having ordinary skill in the art; the Examiner is not entitled to contort the prior art in order to allege that the prior art is thereby interpreted broadly as satisfying the plain meaning of the claim language.

During the telephone interview, the Examiners both seemed to agree that there was no difficulty in the plain meaning of the language of the independent claims. Nor does the rejection currently of record indicate the Examiner "reasonably broad" interpretation of the wording of the claim language.

Rather, the rejections currently of record simply ignore the description in the independent claims that clearly describe that there is a plurality of bonding wires for a signal line and that the configuration of this plurality of bonding wires provides a controlled impedance for that signal line. The rejections currently of record point to a plurality of bonding wires, but this plurality is used for a corresponding plurality of signal lines. The rejections also point to impedance effects in the prior art references, but none of these impedance effects is due to the configuration of a plurality of bonding wires for a specific signal line.

During the above-mentioned telephone interview, as based on the remarks made by the Examiners, the rejection of record rests only upon the interpretation that Kawai can be viewed, in the Examiner's opinion, as teaching a chip wherein there is some sort of impedance matching and that the chip can be presumed as having an input signal on one of the bonding wires 32 and an output signal on another of the bonding wires 31, such that the output signal serves as the return current for the input signal.

The problem with this interpretation of Kawai is that even such strained interpretation of Kawai, clearly not described in any location in Kawai to which the Examiner points in the

rejection, would still fail to satisfy the plain meaning of the claim language, which claim language does not appear to be disputed by the Examiner in the rejection. That is, even the original claim limitations of the independent claims require that the Examiner be able to point out a specific signal line having a plurality of bonding wires, the plurality of bonding wires configured to provide a controlled impedance effect for that signal line.

At most, the Examiner's strained interpretation of Kawai might provide a serial plurality of bonding wires used for a single signal line, but it would still fail to provide a controlled impedance that is due to the configuration of this plurality of bonding wires. The impedance effects in Kawai are clearly due to other factors, since the impedance effect exists in any signal line regardless of whether, for that specific signal line, there is a corresponding output bonding wire for that signal line considered to be an input signal.

Applicants submit that the prosecution history does not attempt to demonstrate a signal line that satisfies the plain meaning of this description and makes no attempt to explain what "broadest reasonable interpretation" the Examiner is giving the claim language.

Instead, the rejection merely attempts to take bits of description out of the context of the prior art references to thereby construct a contorted interpretation of the prior art that is then alleged to match the claim description. Applicants submit that such analysis is not an application of "broadest reasonable interpretation" of the claim language; rather, it is an improper attempt to make a "broadest reasonable interpretation" of the prior art references that is neither confirmed by the description of the prior art references themselves nor an application of the "broadest reasonable interpretation" of claim language.

As such, the rejection currently of record simply fails to meet the initial burden of a *prima facie* rejection, since the plain meaning of the claim language is not satisfied by contorting the teachings of the prior art references until they are deemed to match the claim language. Applicants submit that newly-cited Kawai actually brings nothing of merit to the analysis of the previous Office Action, based on Horiuchi and Notani, which serve as primary references in the latest rejection that includes Kawai as a secondary reference.

That is, on page 4 of the Office Action dated June 19, 2006, the Examiner states: "*Kawai discloses input and output circuits connected by a plurality of bonding wires, in connections with transmission lines which control the impedance of the corresponding circuit (Kawai, col. 2, lines*

40-51 and col. 8, lines 30-52). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the invention of Horiuchi to include the signal and return impedance controls of Kawai in order to produce a high performance semiconductor device and avoid an impedance mismatch caused by different lengths of bonding wires (Kawai, col. 1, lines 60-67)."

However, Applicants submit that the wirebonds in Kawai's patent are all parallel connections where the "plurality" of wirebonds are used in a ganged parallel configuration to minimize the impact of their parasitic inductance on the performance of the impedance matching networks. A key distinction is that one having ordinary skill in the art would consider that the wirebonds in Kawai are all carrying the signal currents and none of them are conveying return currents. The configuration of wirebonds in Kawai are not intended to provide a "controlled impedance" effect in and of themselves, but are part of a larger impedance matching structure. Furthermore, the "return impedance controls" the Examiner mentions are part of a ground plane which conveys the return current. The wirebonds themselves in Kawai do not perform this function, as required by the plain meaning of the independent claims.

On page 8, the Examiner states: "*Kawai discloses input and output circuits connected by a plurality of bonding wires ....*"

However, it is noted that Kawai fails to overcome the deficiencies of Notani. As the Examiner admits: "Notani lacks disclosure specifically of both a signal and return current conducted through the bonding wires ...." As explained above, Kawai does not overcome this deficiency. The return currents in Kawai are not conveyed by the bonding wires, as this is done by a reference ground plane in what is overall a microstrip configuration. The Examiner seems to be confusing "input and output" for "signal" and "return."

Applicants submit that the technique in primary references Horiuchi or Notani (or, for that matter, any of the prior art currently of record) fails to teach or suggest the method of the present invention of using a plurality of bonding wires configured to provide a controlled impedance effect.

As requested in the telephone interview, Applicants respectfully request that the Examiner point to a specific signal line in the prior art references, such that this signal line has a plurality of bonding wires that are configured to provide a controlled impedance effect.

Hence, turning to the clear language of the claims, in Horiuchi there is no teaching or suggestion of: "A method of making an electronic interconnection, said method comprising: for a signal line to be interconnected, using a plurality of bonding wires configured to provide a controlled impedance effect", as required by independent claim 1. Other independent claims have similar language.

Thus, Applicants submit that there are elements of the claimed invention that are not taught or suggested by Horiuchi or Notani or Kawai, and, since the rejection currently of record relies upon these primary references for all pending claims, all claims are clearly patentable over Horiuchi or Notani. Therefore, the Examiner is respectfully requested to withdraw the rejections based on these references.

V. FORMAL MATTERS AND CONCLUSION

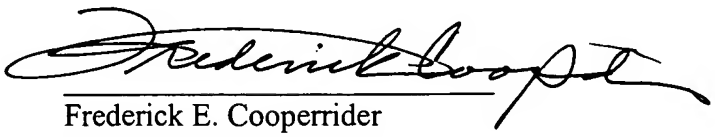
In view of the foregoing, Applicant submits that claims 1-24 and 27-32, all the claims presently being examined in the application, are patentably distinct over the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary in a telephonic or personal interview.

The Commissioner is hereby authorized to charge any deficiency in fees or to credit any overpayment in fees to Assignee's Deposit Account No. 50-0510.

Respectfully Submitted,

Date: 9/19/06



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